RF-SoC—Expectations and Required Conditions

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Invited Paper

***Abstract*—This paper discusses the expectations for the development of radio-frequency systems-on-chip (RF-SoCs) that integrate RF, analog, and digital circuits, and the conditions under which they can be realized. Future RF systems will be increasingly large and complex. However, high integration technology is expected to reduce the circuit size, number of components, and total system cost. Over the past few years, rapid progress of scaled CMOS technology and the introduction of SiGe technology have improved the performance of silicon RF devices and circuits to meet the requirements for conventional RF applications. The RF-SoC, which may be said to be the ultimate goal for RF systems, is expected to improve silicon RF devices even further. However, before this is possible, strict requirements for system perfection, continuous cost reduction, ease of function and specification change, and process portability issues must be resolved. Difficulty in lowering power consumption of RF and analog circuits and of reducing the size of passive components and analog transistors diminish the appeal of the RF-SoC. The RF-SoC in deep submicrometer technology may be an unreasonable solution for some application areas. System-in-package may be one way to address this issue.**

***Index Terms*—CMOS, mixed-signal technology, packaging technology, RF, silicon, system-on-chip.**

I. Introduction

RF SYSTEMS have progressed remarkably with the popularization of cellular phone handsets. This progress will continue in the future because of advancements in RF silicon systems. RF technology is stepping into the market, primarily because of RF networking. Table I summarizes the main features in cellular phone systems; global system for mobile communication (GSM), personal digital cellular (PDC), and IMT2000 and RF network systems; Bluetooth, wireless 1394, IEEE 802.11b, and IEEE 802.11a. RF networking standards have been proposed requiring lower reception sensitivity and transmission power than cellular phone systems. RF networks must serve more devices, about ten per person, than cellular phone systems, because RF networks will be implemented in every electronic device. Thus, cost and ease of system implementation must take priority over performance.

This requirement more aggressively reduces the needed number of components in a system. Fig. 1 illustrates this reduction for the RF components and the total system in a cellular phone handset. Despite continuous reduction, much work is still required. Fig. 2 shows the expected system configuration in the next generation of cellular phone handsets. Two types of cellular phone standards, such as IMT2000 and GSM, should be addressed, also, RF networks, such as Bluetooth for inter-device communication and global positioning system (GPS) for global positioning will be needed. With these additional requirements, unless a more advanced integration technology is introduced, the number of components and circuit size will continue to increase. To solve this problem, the technology must shift from conventional discrete components and board-level assembly to chip- or package-level system integration. RF integration on the silicon is the most promising solution for future RF systems.

Fig. 3 shows the circuit configuration in a conventional RF system. The conventional super heterodyne method needs the surface acoustic wave (SAW) bandpass filter for the first IF and phase-locked loop (PLL) and voltage-controlled oscillator (VCO) for the second mixer. These requirements of the external components result in an increased number of components. Developers of the next generation of RF systems should eliminate the external components that are shaded in the figure by developing direct-conversion or low-IF technology. The power amplifier, antenna switch, and low-noise amplifier (LNA) use conventional GaAs technology, which hinders the complete integration of RF systems. To realize radio-frequency systems-on-chip (RF-SoCs), the industry must develop a full integration technology that will include these parts on the silicon.

This paper discusses the conditions under which the semiconductor industry will accept the RF-SoC for the next generation of RF systems.

II. SoC Technology

The term system-on-chip (SOC) has several definitions. It can be a chip that has embedded multifunctional circuits, such as dynamic random access memory (DRAM), flash memory, analog circuits, and logic components. It can also mean a chip that integrates intellectual property (IP) cores and works as a dedicated system or subsystem.

The digital versatile disk (DVD) player, as shown in Fig. 4, is a complicated system containing high-speed analog and digital signal processing, motor servo, error correction, a copy guard, an MPEG video decoder, and an AC-3 audio decoder. The first generation of DVD players required many large-scale integration (LSIs), but that number has decreased with the progress of LSI technology. DVD players can now be composed of one SoC

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TABLE I
MAIN FEATURES OF CELLULAR PHONE SYSTEMS AND RF NETWORK SYSTEMS

Standard	GSM	PDC	IMT2000	Bluetooth	Wireless 1394	IEEE 802.11b	IEEE 802.11a
Frequency (GHz)	0.9/1.8/1.9	0.8/1.4	1.9-2.1	2.4	5.2	2.4	5.2
Data rate (Mbps)	0.27	0.042	1.92	1	70	11	54
Access method	TDMA	TDMA	CDMA	TDMA	TDMA	CSMA/CA	CSMA/CA
Modulation	GMSK	QPSK	QPSK	GFSK	BPSK, QPSK, 16/64 QAM	CCK, BPSK, QPSK	BPSK, QPSK, 16/64 QAM
TX power (mW)	2000	800	250	1/100		100	40
RX sense (dBm)	-108	-100	-116	-70		-80	-82

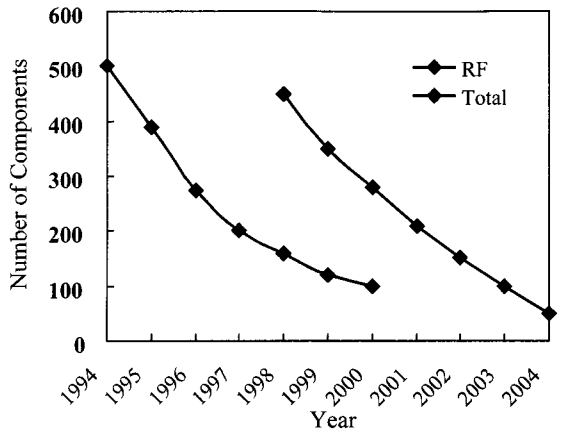

Fig. 1. Reduction of RF components and total components in cellular phone handset.

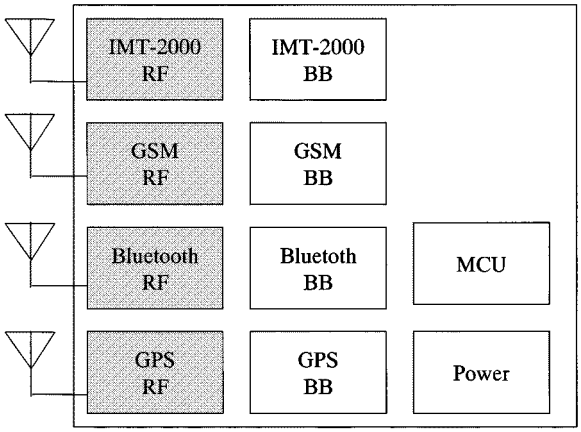

Fig. 2. System configuration in the next-generation cellular phone handset.

and tiny discrete components. Fig. 5 shows a recently developed SoC for use in DVD applications [1]. It contains 24 million transistors and integrates 500-MHz mixed-signal processing circuits, 16-Mb DRAM, and large digital circuits including a 32-b microcontrol unit (MCU) and digital signal processor (DSP). This SoC reduces system cost and increases packing density. Due to this, almost all digital consumer devices now use SoC technology. SoC needs not only ultrahigh integration and embedded technology, but also many IP cores, which means a large circuit block. IP reuse is an important factor for SoC because it shortens development turnaround time (TAT) and reduces cost. SoC technology also requires software for the MCU, DSP, and other digital cores, thus, software development cost is about 50% of the total cost. Fast development TAT and low cost are crucial for success in the SoC business. The following summarizes key factors in SoC success:

1) system reliability and SoC error-free implementation;
2) short TAT;
3) ease of function change;
4) continuous cost lowering with process roadmap;
5) high process portability.

1) System Reliability and SoC Error-Free Implementation: Our study found that more than one-half of the problems with SoC development are due to bugs in the system or system-level verification. If the problem is hardware-related, LSI masks must be changed, which is costly. Hardware bugs also result in longer TAT and possibly loss of business opportunities. System-level verification and LSI circuit verification must be flawlessly executed in a short amount of time. SoC requires system- and circuit-level perfection at a much earlier development stage than conventional system integration, where system bugs are quickly solved by changing the discrete components or low-level integration integrated circuits (ICs). SoC is not the best solution for new systems, but is better for mature systems requiring heavy cost reduction in a huge market.

2) Short TAT: TAT for developing SoCs is longer than that of conventional processes. This is because: 1) long system and circuit verification times are required to assure the systems are bug-free; 2) multiple IP cores and software programs are required, in contrast to board assembly, in which some ICs can be bought from other companies; and 3) processes take much longer to mature because the process is more complex than that of the conventional process. It is crucial that development TAT for SoC be shortened.

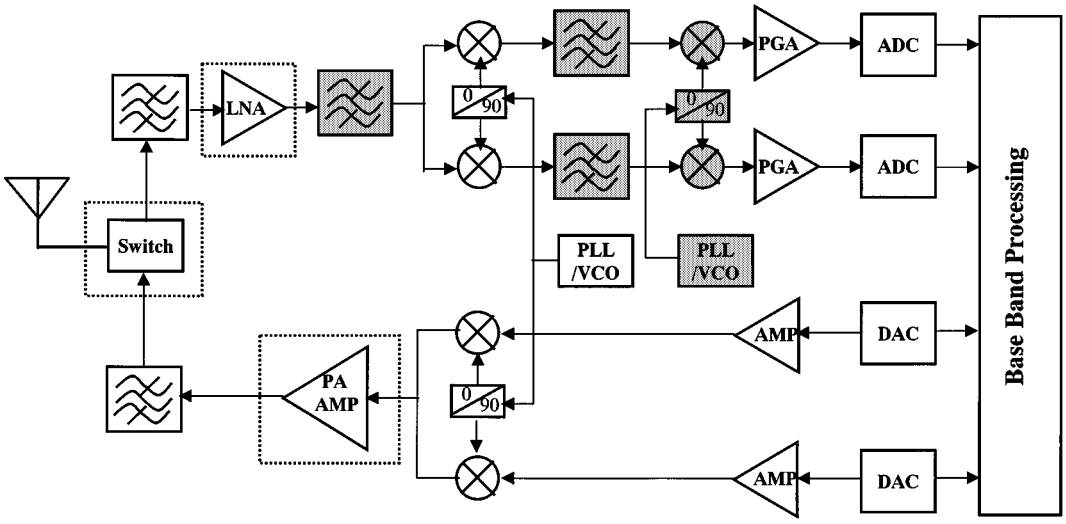

Fig. 3. Circuit configuration in a conventional RF system.

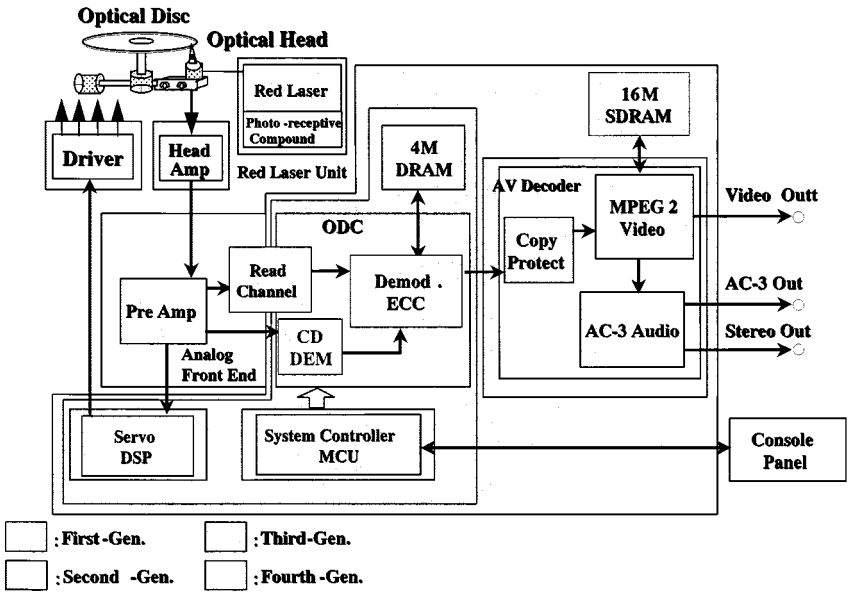

Fig. 4. System configuration of a DVD.

3) Ease of Function Change: SoC is not the proper technology for systems requiring frequent hardware changes. If a hardware change is required, some parts in SoC need to be redesigned and all mask sets changed. This is time consuming and often wastes expensive development fees. To avoid this, the SoC must have changeable software and be programmable. By using technology such as embedded flash, the program can easily be changed late in the development stage or even after the product has shipped.

4) Continuous Decrease in Cost With Process Roadmap: All electric systems demand a continuous decrease in cost. For the silicon digital LSI, device scaling has enabled a continuous cost decrease. Fig. 6 shows several Semiconductor Industry Association (SIA) and International Technology Roadmap for Semiconductors (ITRS) process roadmaps [2]. Up to now, device scaling has progressed and the progress has accelerated. A very important key to the success of the RF-SoC is that this downscaling will allow continuously smaller circuit sizes and improved performance.

5) High Process Portability: A common business strategy is to use multiple fabrication foundries, due to the stable product supply. This requires quick redesigns of the SoC to accommodate different foundry processes, even if the process technology node is the same. Digital circuits require only an adjustment of the propagation delay time to fit different processes. In contrast, analog circuits, particularly RF circuits, are too difficult to redesign to fit all characteristics because analog circuits have multidimensional needed specifications and the design methodology is not clear. Therefore, analog circuits including RF in SoCs must be designed to provide this process portability. How silicon RF technology can or cannot satisfy these conditions will now be discussed.

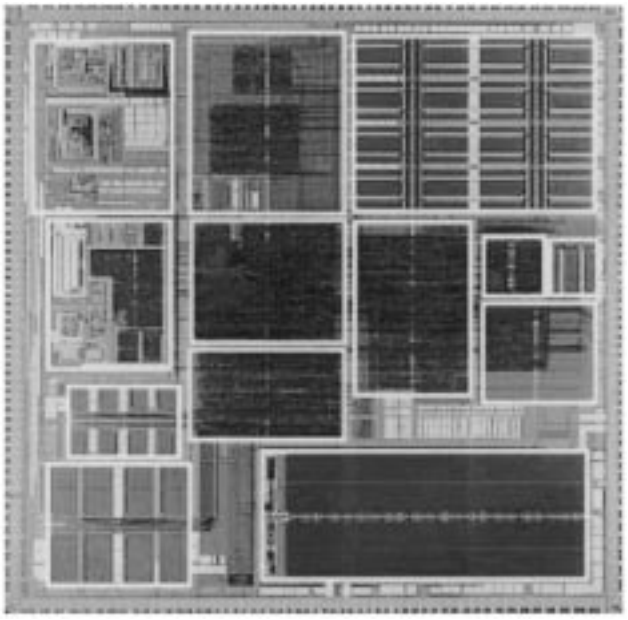

Fig. 5. Chip photograph of SoC for a DVD.

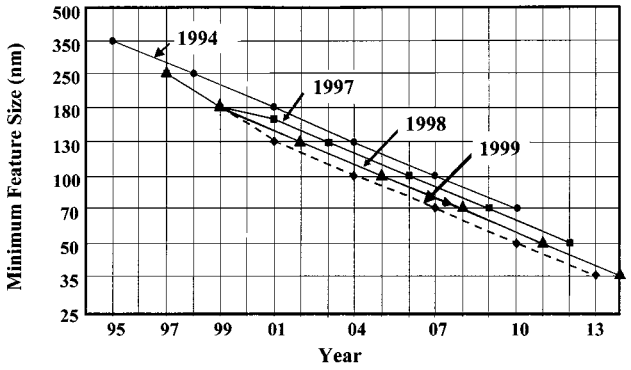

Fig. 6. SIA and ITRS process roadmap in some published years.

III. Silicon RF Technology

GaAs technology has been widely used in RF circuits. If silicon technology can be applied to RF circuits, reduced circuit cost and size are possible because the wafer cost of silicon is much lower than that of GaAs. Furthermore, heavy competition between foundries will further reduce the finished wafer cost. Silicon is the centerpiece in the semiconductor industry and has a large production scale. Fig. 7 shows the percentage of RF and GaAs technology in total semiconductor revenue worldwide [3]. GaAs technology occupies just 1% of the total semiconductor revenue; silicon holds 99%. This suggests that inexpensive resources and aggressive cost lowering by heavy competition are expected when using silicon technology. Six or seven years ago, the RF performance of silicon was insufficient, but today it is worthy of discussion.

Fig. 8 shows the progress of cutoff frequency f_T for several devices. The f_T of bipolar silicon saturated at about 40 GHz, but after the introduction of SiGe technology, has improved to almost 100 GHz. This value is higher than that of conventional GaAs MESFET. The f_T of NMOS was only a few gigahertz, but because of technology scaling, it has increased to approximately

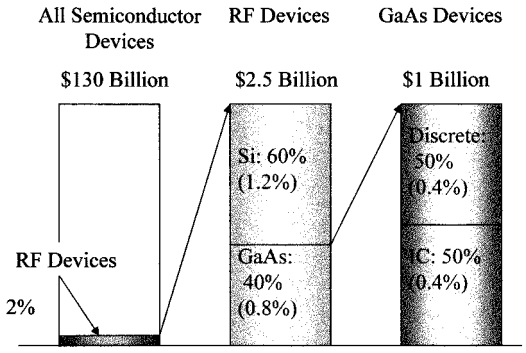

Fig. 7. Occupation of RF and GaAs technologies in the total semiconductor revenue.

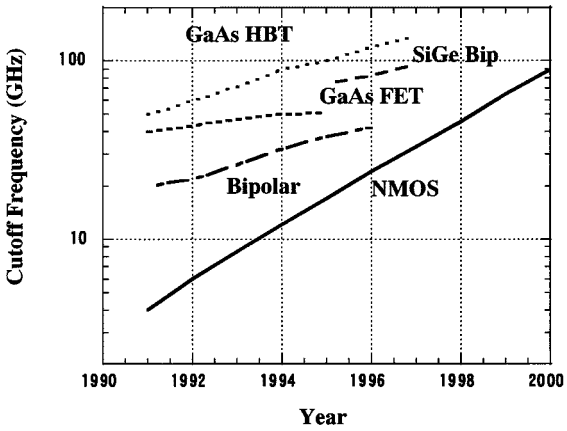

Fig. 8. Progress of cutoff frequency f_T in several devices.

100 GHz at the production level. The cutoff frequency of a GaAs heterostructure bipolar transistor (HBT) is higher than 200 GHz; however, the cutoff frequencies of these silicon devices seem sufficient for mass-market RF applications, whose carrier frequency is a maximum of 5 GHz. This technology change (where the f_T's of silicon devices are higher than 50 GHz) has emerged only during the past few years.

Figs. 9 and 10 show the reported noise figure (NF) of an NMOS LNA [4]–[9] and single-sideband (SSB) phase noise for VCO of silicon devices [10]–[24] in the 1–2-GHz frequency range. The best NF of the LNA is 0.5 dB in SiGe bipolar. The NF for NMOS is insufficient when short channel devices are not used. However, it does improve when short channel devices are used. The best NF in NMOS is less than 1 dB in 0.25-μm technology, and it is comparable to that of SiGe bipolar. The SSB phase noise of a VCO of CMOS devices was insufficient until four years ago. It has now improved, and the recently reported values [10], [11] are better than that of Si or SiGe bipolar.

The current rapid device scaling has contributed to the progress of RF performance in CMOS technology along with the progress of circuit technology. The most essential principle for CMOS technology is a device-scaling rule [25]. The principal scaling rule is to shrink the device dimensions vertically and horizontally, as well as the operating voltage, as shown in Fig. 11. The conventional scale factor is 0.7× for one technology generation. The transistor size is reduced by 0.5× and integration density is increased by 2×. Operating frequency is increased by 1.4×, power consumption

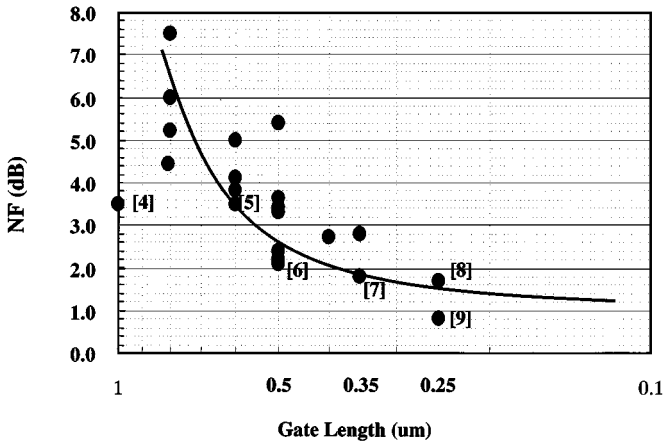

Fig. 9. NF of an NMOS LNA in 1–2-GHz frequency range.

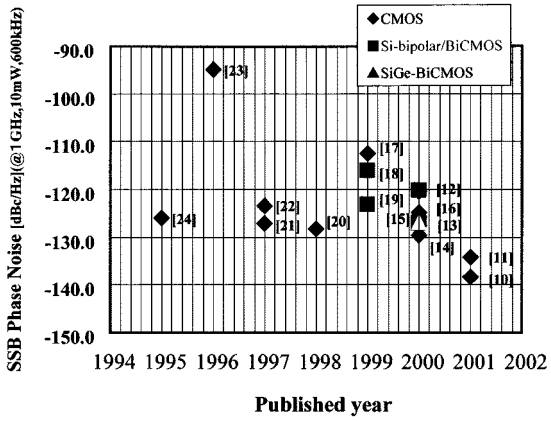

Fig. 10. SSB phase noise for a silicon VCO in 1–2-GHz frequency range.

by about 0.5×, and cost by about 0.7×. This principle helps reduce the chip cost and increase the circuit performance. The essence of CMOS technology development is to accelerate this scaling and to suppress the negative effects due to the nonscalable or antiscalable factors, such as a threshold voltage V_T, resistance and capacitance of interconnections, and contact resistance. This technology that increases the digital circuit performance has also contributed to the improved RF circuit performance. Fig. 12 shows the relationship between current CMOS technology features and performance in digital and RF circuits. Reductions of channel length and gate thickness have contributed to the improvement of f_T, $f\max$, and NF. Salicidation technology, which covers the gate electrode and source and drain area with thin metal films, has been introduced to reduce the digital signal propagation delay and gate, source, and drain resistances. This also has contributed to the improvement of $f\max$ and NF. Cu interconnection technology has been introduced after 0.18-μm technology to decrease the interconnection propagation delay and to increase the electromigration reliability. Currently, thickness of the first or second top interconnection layers are fabricated two or more times thicker to reduce the voltage drop on the power supply line. The number of interconnection layers has been increasing with the progress of technology; thus, the distance between the top interconnection layer and the substrates continues to increase.

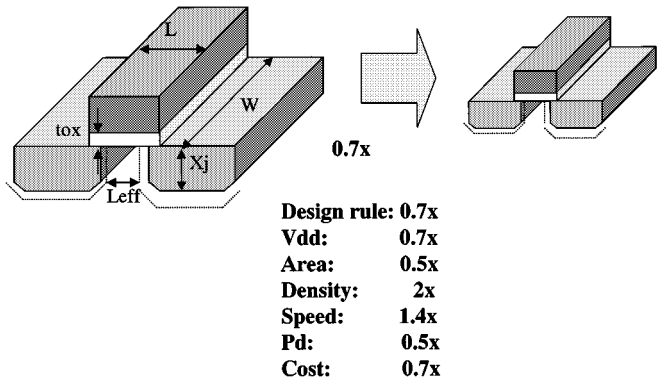

Fig. 11. Principal CMOS scaling rule.

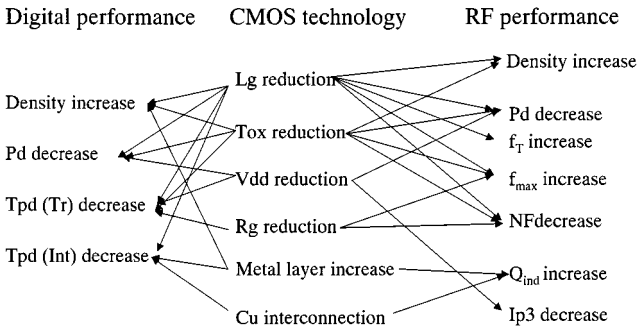

Fig. 12. Relationship between current CMOS technology features and performance progresses in digital and RF circuits.

These trends will contribute to an increase in the quality factor of inductance, which is an essential component for RF circuits.

IV. Design Technology for the RF-SoC

Silicon technology has become useful for application in RF circuits due to the rapid progress of silicon processes and device technologies. To realize the RF-SoC, innovative design technologies are crucial as well.

1) Circuit Technology: Robust direct-conversion or low-IF-conversion technologies are required to eliminate the external filter. It is essential in super-heterodyne conversion and it prevents full-system integration on a chip. There are many issues with direct conversion, such as signal leakage from the local signal to input and the generation of dc offset [26]. However, the issue of dc offset can be addressed by using high-resolution analog-to-digital converter (ADC), with cancellation by digital feedback. Furthermore, dc-offset suppression by a high-pass filter will not cause serious degradation of communication quality for the RF wide-band networking because its signal bandwidth is wide enough.

2) Mixed-Signal System and Circuit Simulation: The RF-SoC is not a component, but a system that achieves needed functions by a combination of RF circuits, analog baseband, and digital signal processing and control. Therefore, the RF-SoC must be designed with total system and circuit simulation. Fig. 13 shows the digital read/write channel system for DVD applications. To optimize the entire system to keep the system strong, the signal processing methods and circuit parameters in the analog and digital circuits, such as the order of filter and

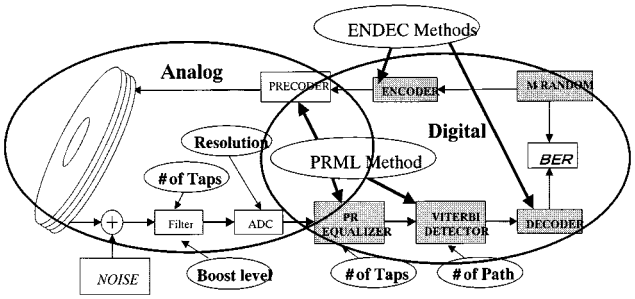

Fig. 13. Digital read–write channel system for DVD application.

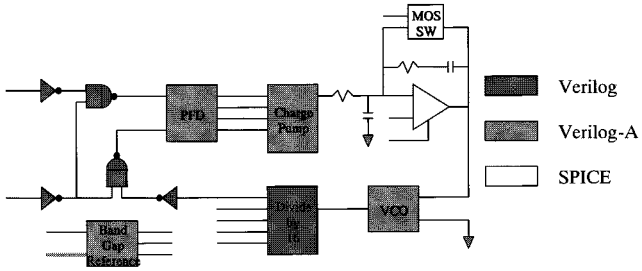

Fig. 14. PLL circuits and simulation methods.

the resolution of ADC, should be optimized concurrently [27], [28]. We simulated a complete system not only under normal conditions, but also under abnormal conditions, by using real DVD signals with C, and C++ language programs, MatLab, and HP-ADS. ADS can generate register transfer level (RTL) for logic synthesis after system simulation. This function guarantees the coincidence between the simulation model and real logic circuits. Circuit simulation has conventionally used SPICE, but this is not suitable for the current analog circuit design. It has an exceptionally long simulation time for several analog or mixed-signal circuits, such as PLL circuits. It has an ultrafast clock signal and a very slow feedback loop, which results in increased simulation time. Fig. 14 shows the PLL circuit and simulation languages [27]. Concurrent mixed-signal simulation with SPICE, digital behavioral language Verilog-D, and analog behavioral language Verilog-A have been used to reduce simulation time up to 50×. The conventional simulation time with SPICE takes about 8 h and the new circuit simulation method takes only 9 min. This simulation time reduction is effective not only in reducing development time, but also in increasing design quality. It enables strong design by using multiple simulations under several operating conditions, such as multitemperatures and process fluctuations.

3) Analog Circuit Synthesis: Sufficient development time can be spent for conventional analog ICs because of infrequent process changes. Current analog circuits in the SoC must be designed quickly to keep up with digital circuits when process changes emerge. New design methodology is needed to address this issue. Analog synthesis, as shown in Fig. 15, is crucial in the future. The needed functions are: 1) selection of circuit topology suitable for realizing the needed function and specification; 2) quick optimization of circuit and device parameters by using accurate device models such as transistors, passive components, interconnections, substrates, and packages; and 3) extraction of an analog behavioral model from the optimized

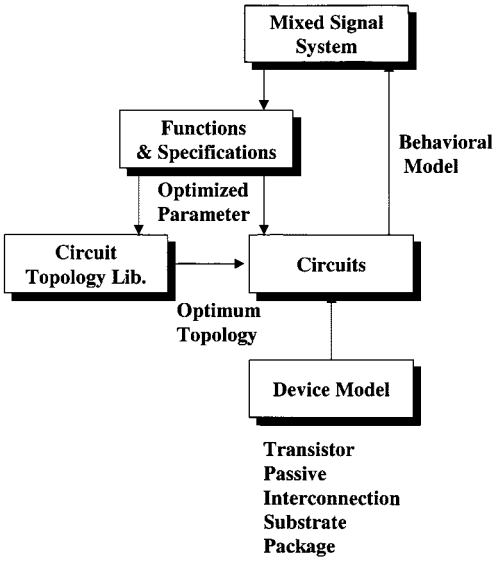

Fig. 15. Analog synthesis.

circuit for system-level simulation. This design methodology can realize fully automated circuit design in order to drastically shorten the design time and increase design quality. Standardization of analog and RF circuits, accurate modeling and extraction of parameters for several devices, and design optimization methodology must be developed. A few years ago, this design method was just a dream for circuit designers, particularly RF designers. Furthermore, MOS device modeling has not addressed RF involving the gate-induced current noise and substrate effect. Current RF MOS circuit design has improved. A design tool for synthesizing the analog circuits including the RF circuit, such as a spiral inductor and VCO, are now available.[1] A new MOS device model, e.g., BSIM4, which involves gate-induced current noise and substrate effect, is in development [29]. Also almost all the silicon foundries can provide RF characteristics of on-chip spiral inductance.

V. RF-SoC and Future Issues

Currently, the silicon RF-SoC can be realized. The technology selection, i.e., SiGe-BiCMOS or CMOS, depends on the application area and needed specification. CMOS technology will be chosen when the specification requirements are low and there is a strong demand for cost reduction. SiGe-BiCMOS technology will be chosen for specifications with higher requirements, especially for sensitivity and low-power consumption, with relatively low priority for cost reduction. The SiGe-BiCMOS has an excellent RF performance; however, the issue is cost and the relatively low performance in digital circuits. The CMOS may have an acceptable performance for RF applications when using 0.25- or 0.18-μm technology, low cost, and relatively high performance in digital circuits. The issues with CMOS are low sensitivity, larger power consumption, and larger mismatch voltage compared with those of SiGe-BiCMOS. The finished wafer price of the SoC is more expensive than that of pure CMOS LSI. This is because the number of steps in the SoC process is increased by several

[1][Online]. Available: http://www.barcelonadesign.com

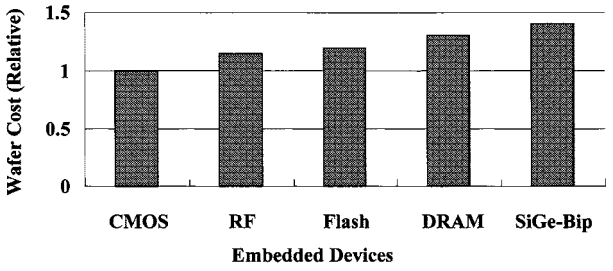

Fig. 16. Finished wafer prices of embedded processes.

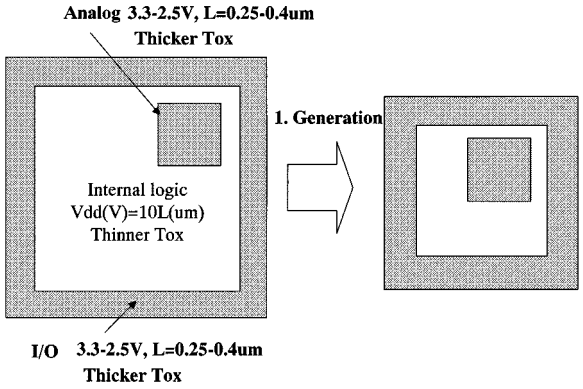

Fig. 17. Chip configuration of a current CMOS SoC.

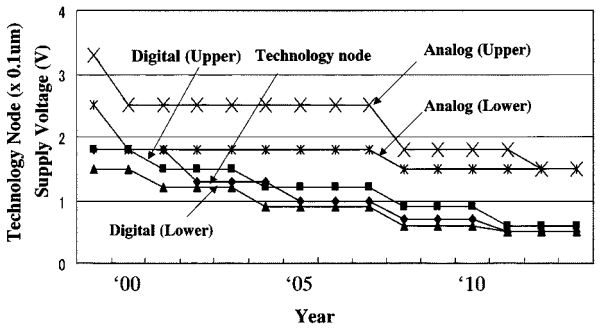

Fig. 18. CMOS technology roadmap.

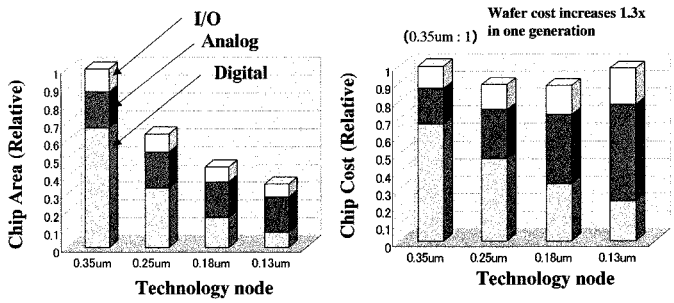

Fig. 19. Estimated chip area and chip cost.

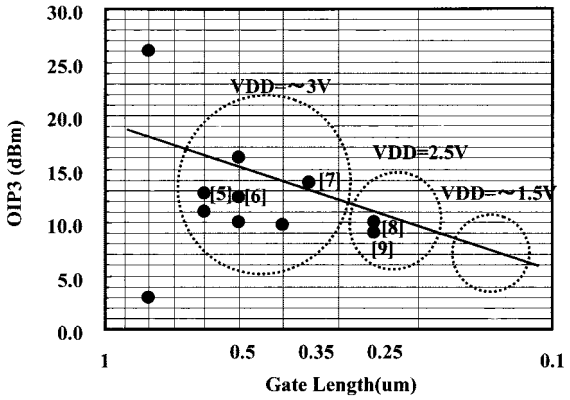

Fig. 20. IOP3 of an NMOS LNA.

nonpure logic functions. RF-SoC needs resistors, metal–insulator–metal (MIM) capacitance, varactors, and inductors that are not needed in logic circuits. Fig. 16 shows the finished wafer prices of embedded processes in 0.25-μm technology. The price increases of RF-CMOS and SiGe-BiCMOS are about 15% and 40%, respectively, compared with the pure CMOS technology. It is easier to design the SiGe-BiCMOS circuits compared with RF-CMOS to obtaining sufficient RF performance with low power consumption. However, the finished wafer price is expensive, and lowering the price will not be easy because of the lack of competition in SiGe-BiCMOS industry compared with the CMOS industry. Thus, if performance is acceptable, CMOS technology is the best choice for the RF-SoC.

The RF-SoC is a possible choice, but it has fundamental business and technology issues. One is a further cost reduction and the other is difficulty in using a more scaled technology. The RF and mixed-signal SoC may embed the nonscalable parts on scalable CMOS logic technology. Nonscalability means performance or cost cannot be improved with technology scaling. It is extremely difficult to reduce the area of analog transistors and passive components. The low mismatch voltage between transistors and the high accuracy or high quality factor for passive components require a larger occupied area. Lowering the voltage of analog circuits causes degradation of the signal-to-noise ratio (SNR), distortion, and tolerance. It also makes it difficult to design the circuits (particularly small-scale devices that provide higher f_T) because device reliability becomes an issue.

Fig. 17 shows the chip configuration for a current CMOS SoC. The chip with a technology node of 0.25 μm or more scaled down has two types of transistors; one is for internal digital circuits and the other is for I/O and analog circuits. The transistor for the internal transistor has thin gate oxide in low operating voltage according to the scaling rule. In contrast, the transistor for I/O and analog circuits has thicker gate oxide with a higher operating voltage such as 3.3 or 2.5 V, as determined by I/O voltage. Fig. 18 shows a CMOS technology roadmap [2]. The operating voltage for digital can be reduced to keep the scaling scenario, however, lowering voltage of analog circuits is more difficult. General-purpose analog and I/O circuits require a voltage between 3.3 and 2.5 V. Some RF circuits can be made with 1.8 or 2.5 V depending on the circuit specifications and functions, researchers are currently studying a more aggressive low-voltage operation. The difficulty in low-voltage operation for RF and analog limits the use of more scaled devices and area reduction. This limitation of area reduction results in an increased chip cost for the SoC. Fig. 19 shows the estimated area and chip cost when the mixed-signal SoC is fabricated in 0.35 μm and the occupied analog circuits occupy 30% of the system, I/O circuits 10%, and digital circuits 60%. If this

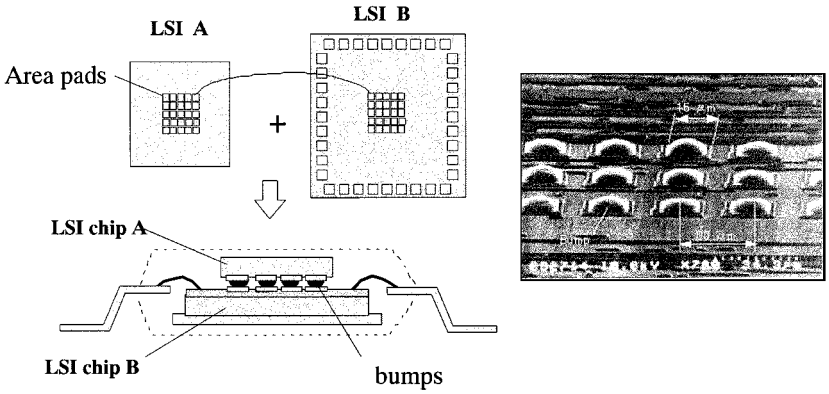

Fig. 21. Package solution.

SoC is fabricated in 0.25-, 0.18-, 0.13-, and 0.1-μm technology, assume that the finished wafer cost will increase 30% for each technology node and that occupied area of the analog and I/O cannot be reduced [28]. The chip size of the SoC can be reduced in each technology node, but the chip cost will increase after the 0.13-μm node. Therefore, a 0.25- or 0.18-μm process is the best choice for this system. This result indicates that the nonscalable parts on an SoC will increase the chip cost when using a smaller scale technology. An occupied area for the RF and analog circuits must be reduced to realize the RF-SoC. The low-voltage operation circuits must be developed to lower the area of transistors; however, it must have the limitation to be 1.5 or 1.8 V. The degradation of dynamic range and increased distortion is a major concern. Fig. 20 shows the output third-order intercept point (OIP3) of an LNA with technology generation [4]–[9]. The distortion has been continuously degraded with technology scaling, thus, the challenge is how to use shorter technology nodes. Novel low-voltage circuit technology, novel compensation or calibration technology to suppress the distortion or degradation of accuracy, and new device technology that can improve the reliability of the device must be developed. Capacitance has an opportunity for scale down by using high dielectric-constant material. However, it will be very difficult to reduce the occupied area for inductance. High-quality inductance will need sufficient area. The design that can reduce the number of passive components to as few as possible is best for the RF-SoC.

VI. System Integration With SiP

The SoC solution may not be the best solution for some RF systems, depending on the required functions, specifications, time, or target cost. However, a conventional board-level solution is no longer acceptable because of the large chip size, high power consumption, and expensive cost. For these systems, a package solution is the best. Fig. 21 shows one candidate for the package solution "system in package" (SiP) [30], [31]. This technology allows you to connect two or more chips or components by microbump bonding with a 30-μm pitch. Capacitance of the connection part is only 10 fF and has no inductance component up to 90 GHz [32]. The 30-μm-pitch connection can provide 1000 contacts in a 1-mm^2 area, which is a sufficient number for conventional use. By using this technology, the most proper technology and design rule for each chip to combine high performance with low cost will be realized. For example, one is a deep submicrometer digital chip and the other is a moderate submicrometer analog and RF chip. This technology allows us to change the functions or specification by changing the analog chip or digital chip quickly. Fig. 22 shows an estimate of total LSI cost when using this SiP technology and using SoC technology. In this case, the analog and I/O circuits use a 0.35-μm CMOS technology and the digital circuits use each technology node. The SoC cannot reduce the cost even if it uses a deeper scaled technology, but the SiP can. Furthermore, the SiP has a feature that can integrate needed nonsilicon components, such as inductances, filters, and large capacitances. A high-Q inductor can be obtained using this technology. The Q of 50 is not unusual for the off-chip inductor [33]; however, the Q for an on-chip inductor is less than 20 at the maximum [34]. This higher Q can reduce the phase noise and power consumption in the VCO [33]. Thus, this SiP solution is an interesting and reasonable solution. SoC and SiP technology shall be developed simultaneously for future RF system-level integration.

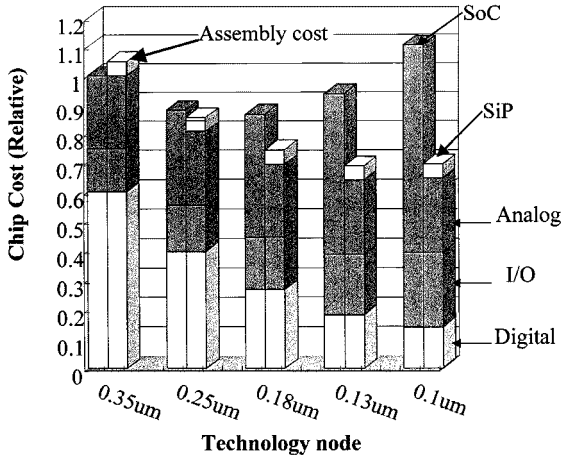

Fig. 22. Estimation of the total LSI cost in the SoC and SiP.

VII. Conclusion

Future RF systems will be increasingly large and complex. However, high-integration technology is expected to reduce the chip size, number of components, and total system cost. Over

the past few years, rapid progress of scaled CMOS technology and the introduction of SiGe technology have improved the performance of silicon RF devices and circuits to meet the requirements for conventional RF applications. The RF-SoC, which may be said to be the ultimate goal for RF systems, is expected to improve silicon devices even further. However, before this is possible, strict requirement for system perfection, continuous cost reduction, ease of function and specification change, and process portability issues must be resolved. Difficulty in lowering power consumption of RF and analog circuits and of reducing the size of passive components and analog transistors diminish the appeal of the RF-SoC. The RF-SoC in deep submicrometer technology may be an unreasonable solution for some application areas. The SiP may be one way to address this issue.

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